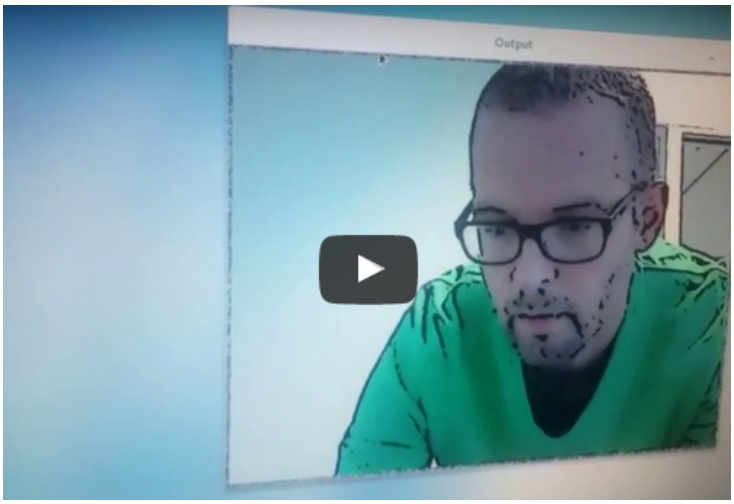
Demo: cartoonizer on an Altera Arria 10 FPGA



It takes quite some effort to program FPGAs using VHDL or Verilog. Since several years Intel/Altera has OpenCL-drivers, with the goal to reduce this effort. OpenCL-on-FPGAs reduced the required effort to a quarter of the time, while also making it easier to alter the specifications during the project. Exactly the latter was very beneficiary when creating the demo, as the to-be-solved problem was vaguely defined. The goal was to make a video look like a cartoon using image filters. We soon found out that "cartoonized" is a vague description, and it took several iterations to get the right balance between blur, color-reduction and edge-detection.

For who has never met me (Vincent Hindriksen), below is a cartoonized video of me trying out the live version of the FPGA-Cartoonizer in the noisy server-room. All credits go to the StreamHPC team, who did the programming!

The demo has been used by EBV to showcase how quick software can be developed when using OpenCL. Even if the final version would be ported to Verilog or VHDL, the total time spent would be far less due to OpenCL's flexibility.

It uses OpenCV for the webcam-stream, CentOS Linux and OpenCL. The lag is due to the limited memory-speed and the OpenCV-overhead. We focused on FPGA-style programming and getting the parameters right, not on getting the maximum performance out by sacrificing readability.

Would you like to see and hear more what we can do with FPGAs? Get in contact.